REMARKS

Present Status of the Application

claims 1-15 are still pending because these claims are rejected based on the new grounds. However, applicant respectfully disagrees the examiner's rejection grounds. Accordingly, the applicant submits the following arguments. For at least the foregoing reason, reconsideration of the claims 1-15 is respectfully requested.

Discussion of the claim rejection under 35 USC 103

3. Claims 1, 5, 6, 9, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray (US 5,373,255, hereinafter, referred as Bray) in view of Lee et al. (US 5,373,255, hereinafter, referred as Lee)

In response thereto, applicants do not agree the above examiner's allegation and provide the following arguments.

First of all, the first requirement for establishing a prima facie case of obviousness is that either of Bray and Lee should teach, suggest or disclose any motive(or need) to modify the prior art references to arrive at the present invention. To cause any one skilled in the art to which the present invention pertains to make such combination, the first requirement is that problems intended to be solved by each prior art reference should be explicitly or implicitly not only addressed and identical each other, but identical to that of the present invention as well. Accordingly, from col.1, lines 59-60, in Bray, there discloses a problem to be solved is that

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unwanted signal jitter occurs in a PLL (phase lock loop) circuit; however, from col. 2, lines 1-4, in Lee, a problem to be solved is that a consider time delay occurs in order the CPU (3) to read data. Furthermore, from line 4, in the paragraph [0002] and the paragraph [0003], the present invention intends to solve a longer phase-locking time problem. Therefore, the problem intended to be solved by Bray and Lee are not identical, and not identical to that of the present invention neither. As a result, there is no desirability (or a motive) disclosed in either Bray and Lee for any one skilled in the art to which the invention pertains to make a combination of Bray and Lee

Even if Bray and Lee could be combined, this combination still fail to reach, suggest or disclose "a phase digital converter for comparing a feedback signal with a feedback frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency, and outputting a digital phase adjusting signal," (emphasis added) as claimed in the claim 1. As the scope of a device in the claim language should be construed as a whole, in Bray, either of a phase detector 41 that outputs an "up" signal and a "down" signal, and a phase error accumulator 42 that receives these two signals and a "sample clock", as well as a "latch clock," can not be construed to be identical to the phase digital converter as claimed in the claim 1. This is because the scope of the phase digital converter as claimed in the claim 1 can not be pieced to be identical to either of the phase detector 41 and the phase error accumulator 42 or the combination thereof as disclosed in Bray. Accordingly, the independent claim 1 is not rendered obvious by Bray and Lee and thus patentable under 35 USC 103(a).

5. Claims 1, 5, 6, 9, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray (US 5,373,255, hereinafter, referred as Bray) in view of Werker et

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al. (US 5,856,762, hereinafter, referred as Werker)

In response thereto, applicants do not agree the above examiner's allegation and provide the following arguments. As stated above, to cause any one skilled in the art to which the present invention pertains to make such combination, the first requirement is that problems intended to be solved by each prior art reference should be explicitly or implicitly not only addressed and identical each other, but identical to that of the present invention as well. From the preceding description, although the problem intended to be solved by Bray and Werker are identical; that is, an unwanted signal jitter occurs in the PLL (phase lock loop) circuit. However, this problem is not identical to that of the present invention, a longer phase-locking time problem. As a result, there is no desirability (or a motive) disclosed in either Bray and Werker for any one skilled in the art to which the invention pertains to make a combination of Bray and Werker. In other words, any one skilled in the art to which the invention pertains won't make a combination of Bray and Werker because this combination is not able to benefit him/her.

As discussed in the preceding section, even if Bray and Lee could be combined, this combination still fail to reach, suggest or disclose "a phase digital converter for comparing a feedback signal with a feedback frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency, and outputting a digital phase adjusting signal," (emphasis added) as claimed in the claim 1. Likewise, the independent claim 1 is not rendered obvious by Bray and Werker and thus patentable under 35 USC 103(a).

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Regarding the dependent claims 2, 4, 8, 12 and 14 objected under 35 USC 103(a), they should be patentable as a matter of law for the reason that they at least contain the limitation of "a phase digital converter," as claimed in their patentable base claim 1.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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